REMARKS/ARGUMENTS

This paper is being provided in response to the October 18, 2004 Office Action for the above-referenced application. In this amendment, Applicant has canceled Claim 5, and amended Claims 1-8 and 30 in order to more particularly point out and distinctly claim that which Applicant deems to be the invention. Applicant respectfully submits that the amendments to the claims are all supported by the originally filed application.

The rejection of Claims 1-17, 22-26, and 30-36 under 35 U.S.C. § 102(b) as being anticipated by Nishikawa et al. (U.S. Patent No. 6,087,261, hereinafter referred to as "Nishikawa") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1-17, 22-26, and 30-36, as amended herein, are patentable over the cited reference. The rejection as applied to Claim 5 is moot in view of the cancellation of Claim 5 herein.

Claim 1 recites a method for forming a semiconductor device having a laminated structure including a dielectric film made from a metal oxide formed on a surface of a heated substrate and a CVD high melting point metal nitride film, wherein said metal nitride film is directly formed on said dielectric film by introducing a source gas containing said high melting point metal into a chamber in which said substrate is contained, said method comprising a step of heating said substrate while adding NH_3 gas, and, after said heating, adding to the NH_3 gas a non-reactive ambient having no component that reacts with said metal oxide formed on said surface of said substrate in said chamber, wherein said non-reactive ambient includes a member of the group consisting of a gas non-reactive with respect to said metal oxide contained in said

dielectric film, and introducing into said chamber a source gas for forming said CVD-TiN film and NH_3 gas, following said heating step, and further wherein a temperature of said substrate is set at a prescribed temperature, before said source gas containing said high melting point metal is introduced into said chamber. Claims 2-4, 6, 7, 11, and 13-17 depend from Claim 1.

Claim 8 recites a method for forming a semiconductor device having a laminated structure of a dielectric made from a metal oxide and a CVD high melting point metal nitride film formed thereover, wherein said metal nitride film is directly formed on said dielectric film by introducing a source gas containing said high melting point metal into a chamber in which said dielectric film is contained, said method comprising; heating a substrate onto which said dielectric film is formed to a prescribed temperature and, during said heating, adding NH_3 gas, and, after said heating, adding to the NH_3 gas an ambient at a partial pressure no greater than 1.0 Torr and no less than 0.1 Torr before the introduction of said source gas containing said high melting point metal, wherein said NH_3 gas does not react with said dielectric film. Claims 9-10 and 22-26 depend from Claim 8.

Claim 30 recites a method for forming a CVD-TiN film, wherein a titanium nitride (TiN) film is formed on a dielectric film that includes an oxide material formed by a CVD film forming process within a CVD film forming device, said method comprising: heating a substrate provided with said dielectric film in said CVD film forming device while adding NH_3 gas, and, after heating, adding to the NH_3 gas an atmosphere having no component which reacts with said dielectric film including said oxide material; and forming said titanium nitride (TiN) film on said dielectric film in said CVD film forming device. Claims 31-36 depend from Claim 30.

Nishikawa discloses a method of producing a semiconductor device. (See Col. 1, Lines 7-10 and Abstract). Nishikawa discloses formation of a titanium nitride film. After the silicon substrate has been placed on the lower electrode inside the reaction chamber of the CVD device, the interior of the reaction chamber is decompressed and the heater is turned on to set the temperature of the substrate at 500° C. After the substrate temperature has been set at 500° C, the O_2 gas and the He gas are supplied. After the elapse of 30 seconds following the start of the supply of oxygen and helium, NH_3 and MMH gases are introduced into the chamber. (Col. 8, Line 58-Col. 9, Line 37; Col. 10, Lines 14-31).

Applicant's Claim 1 is neither disclosed nor suggested by Nishikawa in that Nishikawa neither discloses nor suggests heating the substrate while adding NH_3 gas, and, after the heating, adding to the NH_3 gas a non-reactive ambient as set forth in amended Claim 1. As pointed out above, Nishikawa discloses first heating the substrate, then adding O_2 and He, and then adding NH_3. Nishikawa neither discloses nor suggests heating the substrate while adding NH_3 gas as set forth in Applicant's claim 1.

For reasons similar to those set forth regarding Claim 1, Claim 8 is neither disclosed nor suggested by Nishikawa in that Nishikawa neither discloses nor suggests at least the feature of heating the substrate to a prescribed temperature and, during the heating, adding NH_3 gas, and, after the heating, adding to the NH_3 gas an ambient at a partial pressure no greater than 1.0 Torr and no less than 0.1 Torr before the introduction of a source gas containing the high melting point metal, as set forth in Claim 8.

For reasons similar to those set forth regarding Claim 1 and Claim 8, Claim 30 is neither disclosed nor suggested by Nishikawa in that Nishikawa neither discloses nor suggests at least the feature of heating a substrate having a dielectric film in a CVD film forming device while adding NH_3 gas, and, after heating, adding to the NH_3 gas an atmosphere having no component which reacts with the dielectric film including an oxide material, as set forth in Claim 30.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 1-4, 11, 13-17, 19-20 and 30-31 under 35 U.S.C. § 102(b) as being anticipated by Tamaru et al. (U.S. Patent No. 6,103,566, hereinafter referred to as "Tamaru") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that 1-4, 11, 13-17, 19-20 and 30-31 are patentable over the cited reference.

Claim 1 is summarized above. Claims 2-4, 11, 13-17, and 19-20 depend from Claim 1.

Claim 30 is summarized above. Claim 31 depends from Claim 30.

Tamaru discloses use of a titanium-containing source gas, a nitrogen containing reducing gas, and an inert gas. The gases are introduced into the chamber of the CVD apparatus of Figure 35. The inert gas is introduced while raising the temperature of the substrate. When the substrate temperature becomes substantially constant, the titanium containing source gas is introduced and thermally decomposed to form a passivation film 78. Subsequently, the nitrogen containing

reducing gas is introduced into the chamber and reacted with the titanium containing gas thereby to deposit a TiN film over the surface of the passivation film 78. The titanium containing source gas may be introduced substantially simultaneously with the inert gas while the temperature of the substrate is raised, as shown in Figure 39, or just before the introduction of the nitrogen containing reducing gas, as shown in Figure 40. In either case, however, the titanium containing source gas is introduced prior to the introduction of the nitrogen containing reducing gas. (Figures 35-40; Col. 16, Lines 15-51).

Applicant's Claim 1 is neither disclosed nor suggested by Tamaru in that Tamaru neither discloses nor suggests heating the substrate while adding NH_3 gas, and, after heating, adding to the NH_3 gas a non-reactive ambient, as set forth in amended Claim 1. Tamaru discloses adding an inert gas and a Ti-containing gas during a temperature raising step, but Tamaru appears silent regarding any disclosure or suggestion of adding NH_3 gas during a heating step. Accordingly, Tamaru neither teaches, discloses or suggests features of Applicant's amended Claim 1.

For reasons similar to those disclosed regarding Claim 1, Applicant's Claim 30 is neither disclosed nor suggested by Tamaru in that Tamaru neither discloses nor suggests heating a substrate provided with a dielectric film in a CVD film forming device while adding NH_3 gas, and, after heating, adding to the NH_3 gas an atmosphere having no component which reacts with the dielectric film including an oxide material, as set forth in Claim 30.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 18-21 and 27-29 under 35 U.S.C. § 103(a) as being unpatentable over Nishikawa in view of Kang, et al. (U.S. Patent No. 6,139,700, hereinafter referred to as "Kang") and Asano et al. (U.S. Patent No. 6,268,985, hereinafter referred to as "Asano") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 18-21 and 27-29 are patentable over the cited reference.

Claims 18-21 depend from Claim 1 and Claims 27-29 depend from Claim 8. For reasons set forth above, Claims 1 and 8 are neither disclosed nor suggested by Nishikawa. For reasons set forth below, Applicant respectfully submits that combining Nishikawa with Kang and Asano also neither discloses nor suggests Applicant's Claim 1 and 8, and claims that depend therefrom.

Kang discloses a method and apparatus of fabricating a metal interconnection in a contact hole of a semiconductor device. (See Abstract; Col. 1, Lines 8-11). In Figure 1B of Kang, Kang discloses a protective layer 18 formed on a Ti layer 16 before forming an ALD metal barrier layer 20. The protective layer includes a metal nitride layer and is formed by nitriding an upper surface of the Ti layer 16. (Col. 4, Lines 24-32).

Asano relates to a semiconductor integrated circuit device and a method of manufacturing the same. The semiconductor integrated circuit device has a DRAM including a memory cell portion formed at a first portion of a main surface of a semiconductor substrate and a peripheral circuit portion formed at a second portion of the main surface. Asano discloses that bit line conductors are disposed in the memory cell region and first level interconnect conductors are disposed in the peripheral circuit region, and exist at the same level. (See Abstract; Col. 1, Lines

11-19; Col. 2, Lines 23-26). Asano discloses that the thickness of the bit line and the thickness of a conductor film constituting the interconnect conductor of the peripheral circuit portion must be optimized. (Col. 2, Lines 34-37).

Asano and Kang appear silent with regard to any disclosure or suggestion of the features of Applicant's Claim 1, Claim 8, and Claim 30 not found in Nishikawa. Thus, combining Nishikawa with Asano and Kang does not overcome the deficiencies of Nishikawa with respect to Applicant's independent claims.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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Date

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